WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a trench on a surface; and

an MIS (Metal Insulator Semiconductor) transistor including a source region formed to face said surface in said semiconductor substrate, a drain region formed to face said surface in said semiconductor substrate apart from said source region through said trench, a gate insulating film formed on at least a portion of said surface which is interposed between said source region and said drain region to enter said trench, and a gate electrode formed on said gate insulating film to enter said trench,

wherein first and second electric charge holding portions capable of holding an electric charge are formed in said gate insulating film to interpose said trench therebetween.

2. The semiconductor device according to claim 1,

wherein said gate insulating film is a laminated film in which a first silicon oxide film, a silicon nitride film and a second silicon oxide film are sequentially provided, and

said first and second electric charge holding portions are first and second portions in said silicon nitride film which interpose said trench therebetween and are opposed to each other.

3. The semiconductor device according to claim 1,

wherein said first and second electric charge holding portions are not formed in a portion of said gate insulating film which enters said trench.

4. The semiconductor device according to claim 1,

wherein another MIS transistor having another source region, another drain region, another gate insulating film and another gate electrode is also formed on said semiconductor substrate.

5. The semiconductor device according to claim 4,

wherein said first and second electric charge holding portions are not formed in a portion of said gate insulating film which enters said trench and said another gate insulating film of said another MIS transistor is extended in said portion of said gate insulating film which enters said trench.

6. The semiconductor device according to claim 1,

wherein said first and second electric charge holding portions have ends on said source region and said drain region.

7. The semiconductor device according to claim 6,

wherein insulating films for covering said ends of said first and second electric charge holding portions are formed on said ends, respectively.

8. The semiconductor device according to claim 1,

wherein corner portions of an upper end and a bottom in said trench are rounded.

9. The semiconductor device according to claim 1,

wherein said first and second electric charge holding portions are formed by a

plurality of insular regions formed in said gate insulating film.

10. The semiconductor device according to claim 9,

wherein said insular regions are constituted by silicon or a silicon nitride film.

11. The semiconductor device according to claim 1,

wherein said first and second electric charge holding portions are formed in said gate insulating film which is adjacent to a side surface of said trench.

12. A semiconductor device comprising:

a semiconductor substrate having a surface; and

an MIS (Metal Insulator Semiconductor) transistor including a source region formed to face said surface in said semiconductor substrate, a drain region formed to face said surface in said semiconductor substrate apart from said source region, a gate insulating film formed on at least a portion of said surface which is interposed between said source region and said drain region, and a gate electrode formed on said gate insulating film,

wherein first and second electric charge holding portions capable of holding an electric charge are formed in said gate insulating film opposite to each other in such a direction as to connect said source region and said drain region apart from each other,

a thickness of a portion of said gate insulating film which is interposed between said first and second electric charge holding portions is smaller than that of each of portions in which said first and second electric charge holding portions are formed, and

said gate electrode is provided between said first and second electric charge holding portions.

13. The semiconductor device according to claim 12,

wherein both of said first and second electric charge holding portions are silicon nitride films, and

a first silicon oxide film, said silicon nitride film and a second silicon oxide film are provided on said semiconductor substrate in this order.

14. The semiconductor device according to claim 13,

wherein said portion of said gate insulating film which is interposed between said first and second electric charge holding portions is an extended portion of said first silicon oxide film.

15. The semiconductor device according to claim 12,

wherein insulating films are formed between ends of said first and second electric charge holding portions which are opposed to each other and said gate electrode.

16. The semiconductor device according to claim 12,

wherein said first and second electric charge holding portions have other ends on said source region and said drain region, respectively.

17. The semiconductor device according to claim 16,

wherein insulating films for covering said other ends of said first and second electric charge holding portions are formed on said other ends, respectively.

18. The semiconductor device according to claim 12,

wherein both of said first and second electric charge holding portions are

formed by a plurality of insular regions in said gate insulating film.

19. The semiconductor device according to claim 18,

wherein said insular regions are constituted by silicon or a silicon nitride film.